A Stacked DRAM Solid State Recorder Using a Novel Laser 3D Interconnect Process

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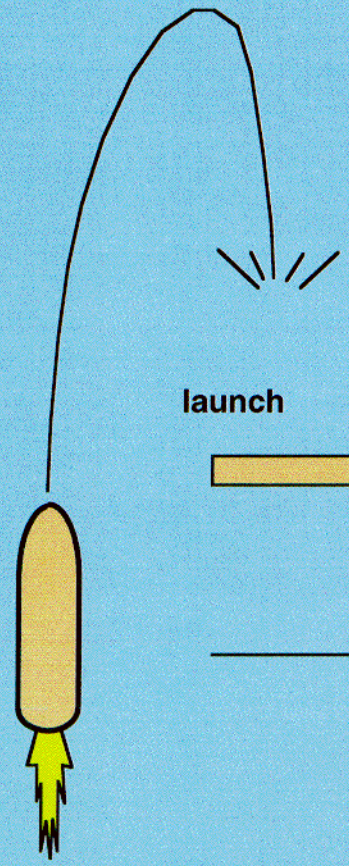
Presentation Outline

- Solid state memory module for “high fidelity” ICBM flight tests
  - Flight test overview
  - Telemeter configuration
  - Solid state recorder architecture
- Overview of memory module fabrication
- Front-end of process - rerouting I/O pads to chip sidewall
  - 3D laser patterning
    - Electrodeposited photoresist
    - Metallization
- Back-end of process - connection to next level of packaging
  - Bonding DRAM stack to flex circuit
  - Bonding stack-on-flex to PCB
- Summary

High Fidelity Flight-Test Microtelemetry

- Transmit sensor data on flight and device dynamics
- Minimize telemeter impact on data by reducing size and weight
- Eliminate need for midrange receiving stations by storing data to memory before horizon break



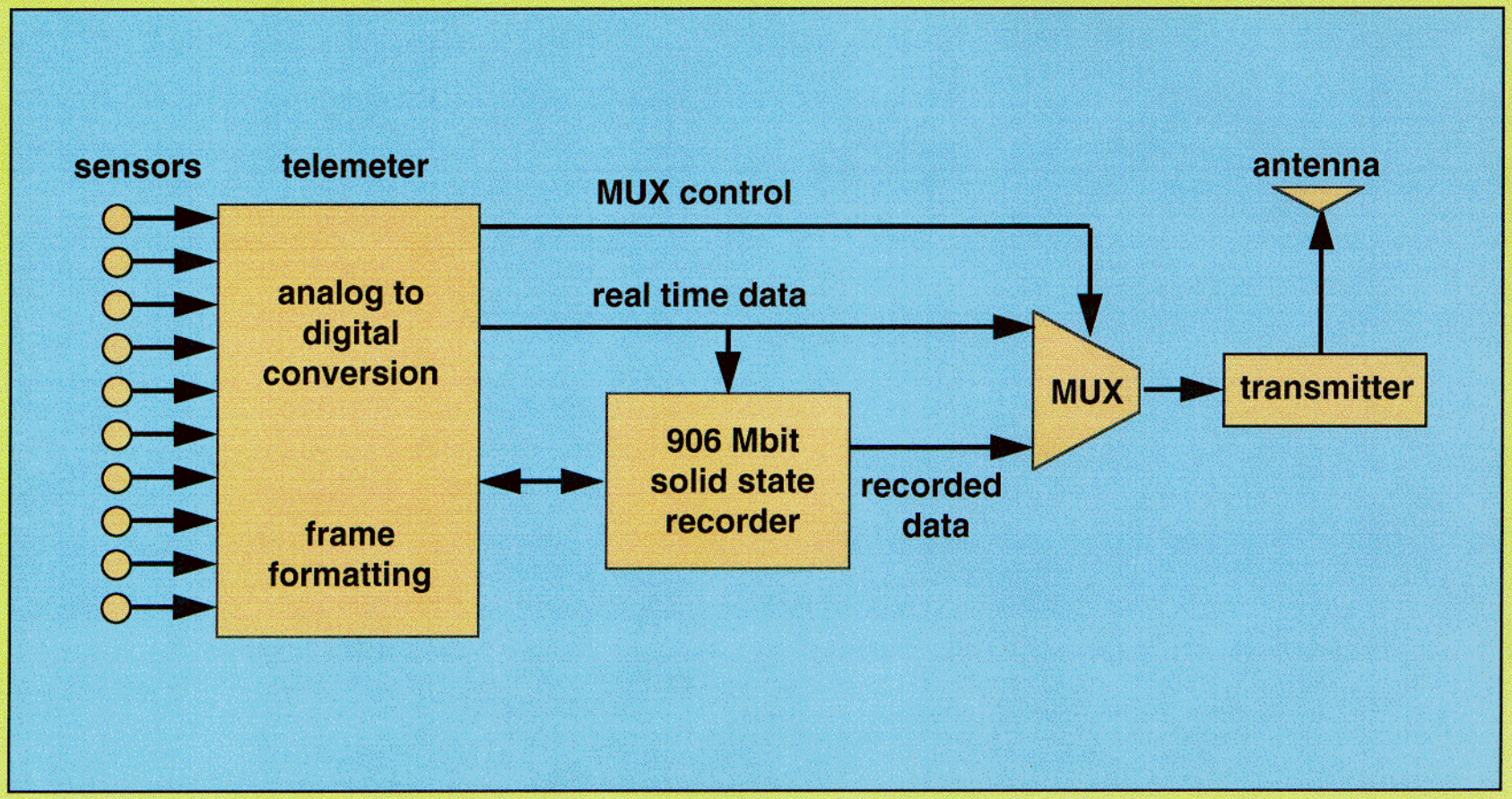
launch horizon break splash

transmit recorded data transmit real time

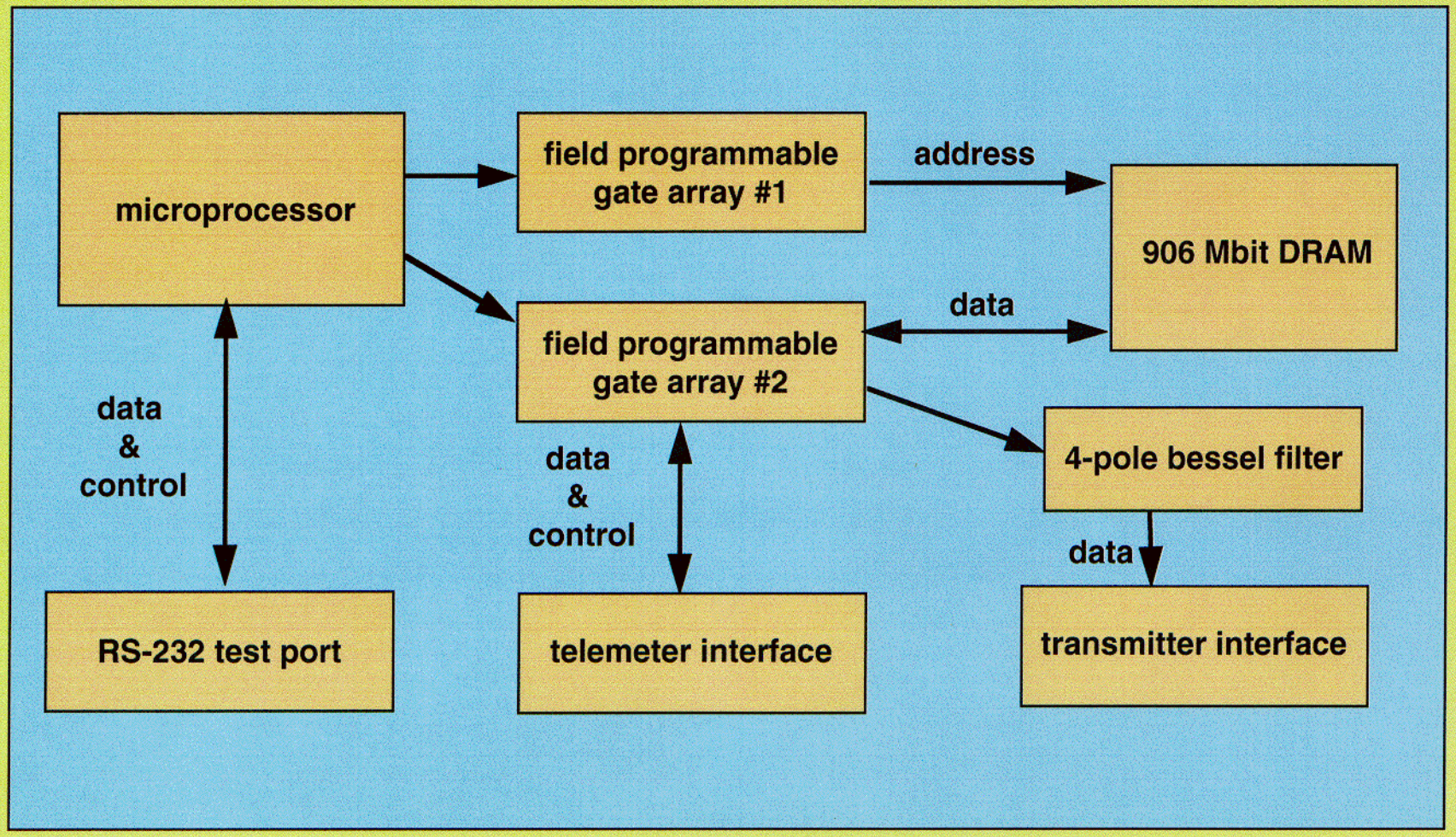
record data to memory

~1 Gb memory needed for 30 min flight test

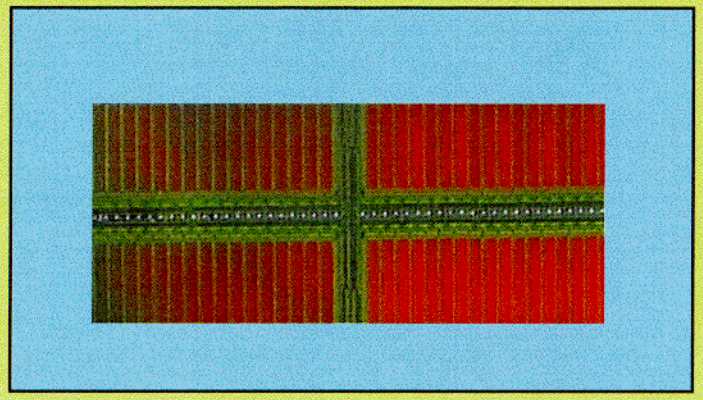
Telemeter Configuration with Memory



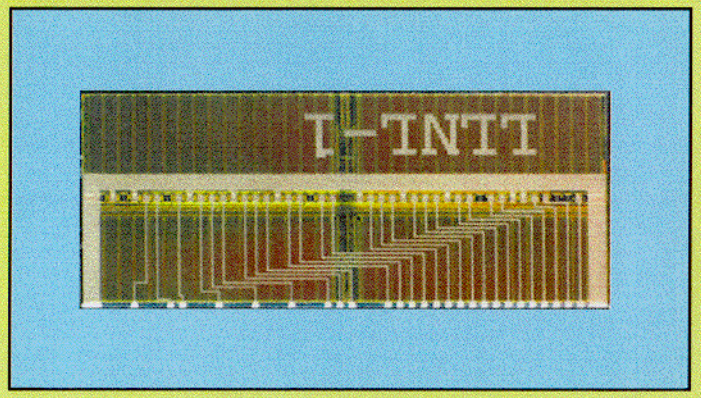
Solid State Recorder Architecture



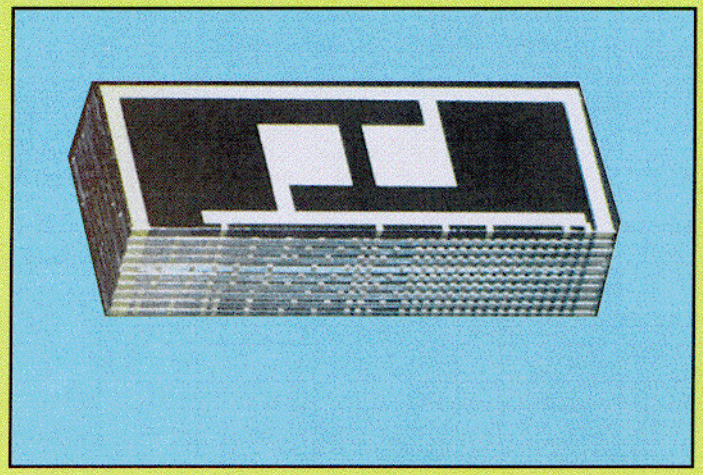
Overview of DRAM Reroute and Stacking Process



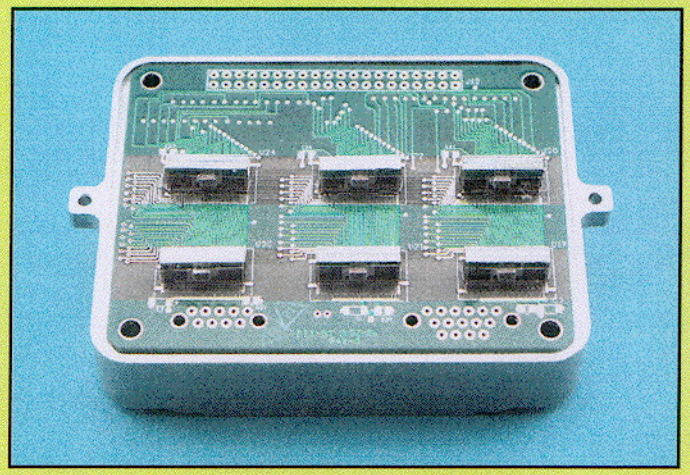
TI 16 Mb DRAM (4M x 4)



DRAM after laser reroute

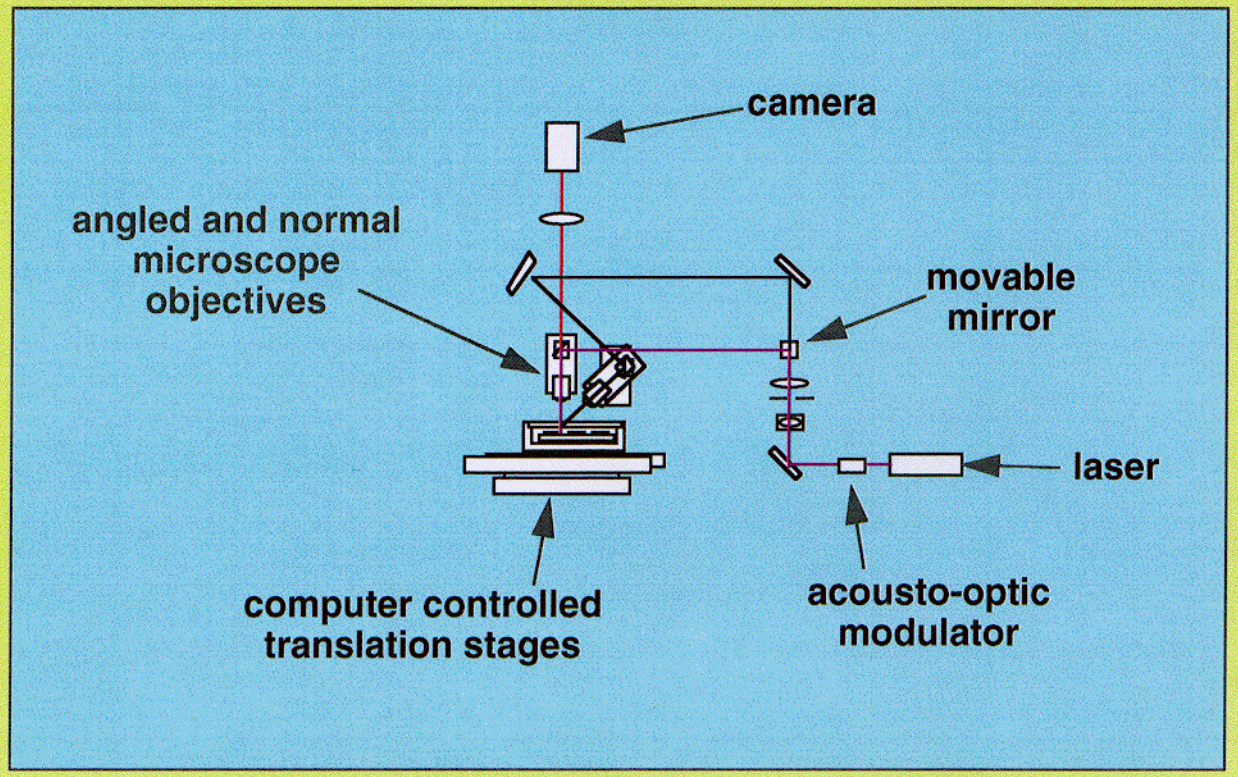


9-DRAM 144 Mb stack

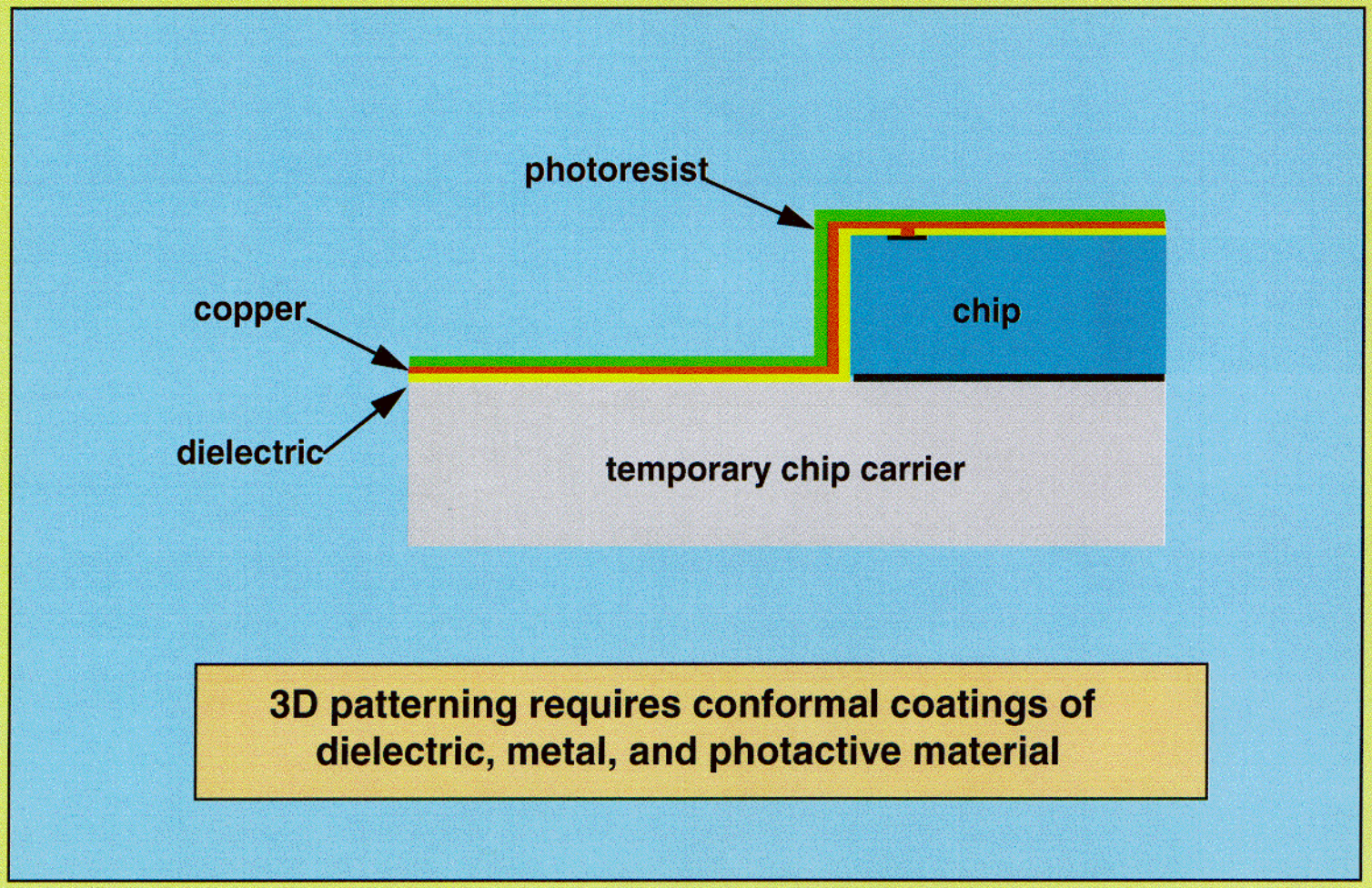


906 Mb memory board

Laser Tool For Patterning Vertical As Well As Horizontal Surfaces

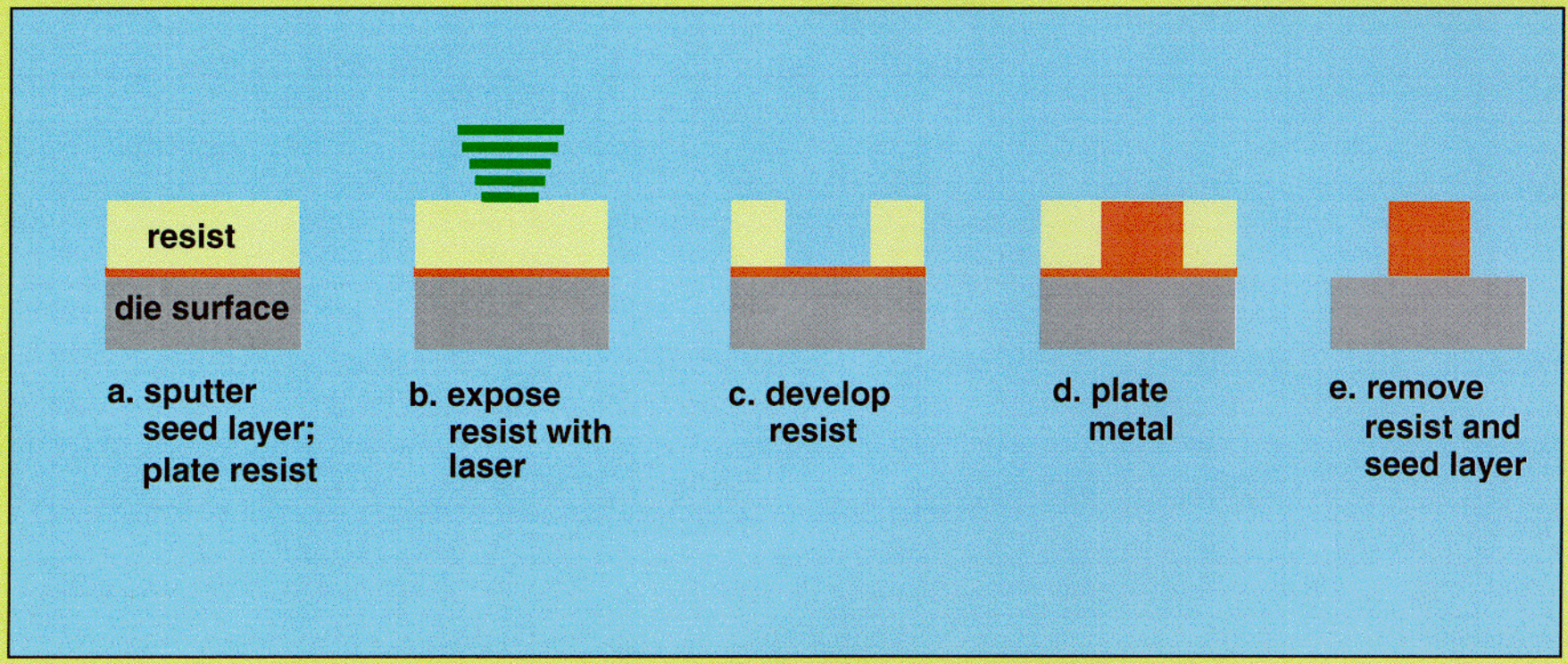


Unique Requirements for Laser 3D Patterning

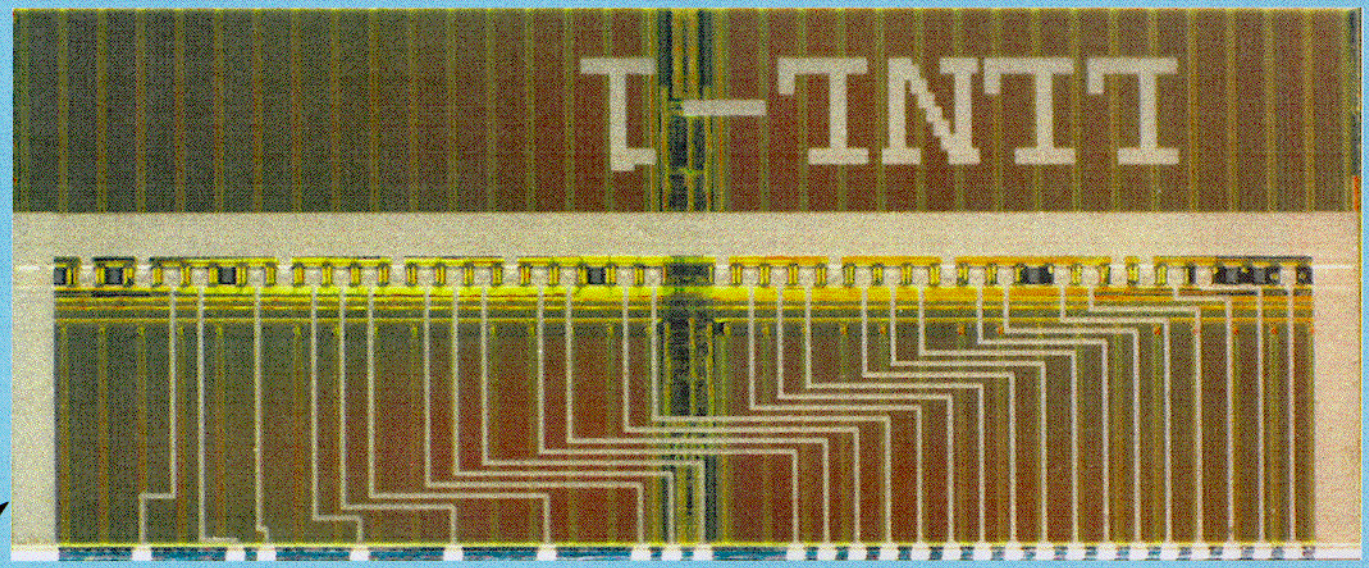


3D patterning requires conformal coatings of dielectric, metal, and photactive material

Overview of Laser Reroute Process Using Positive Electrodeposited Photoresist



Reroute Pattern is Unique for Each Die in Stack



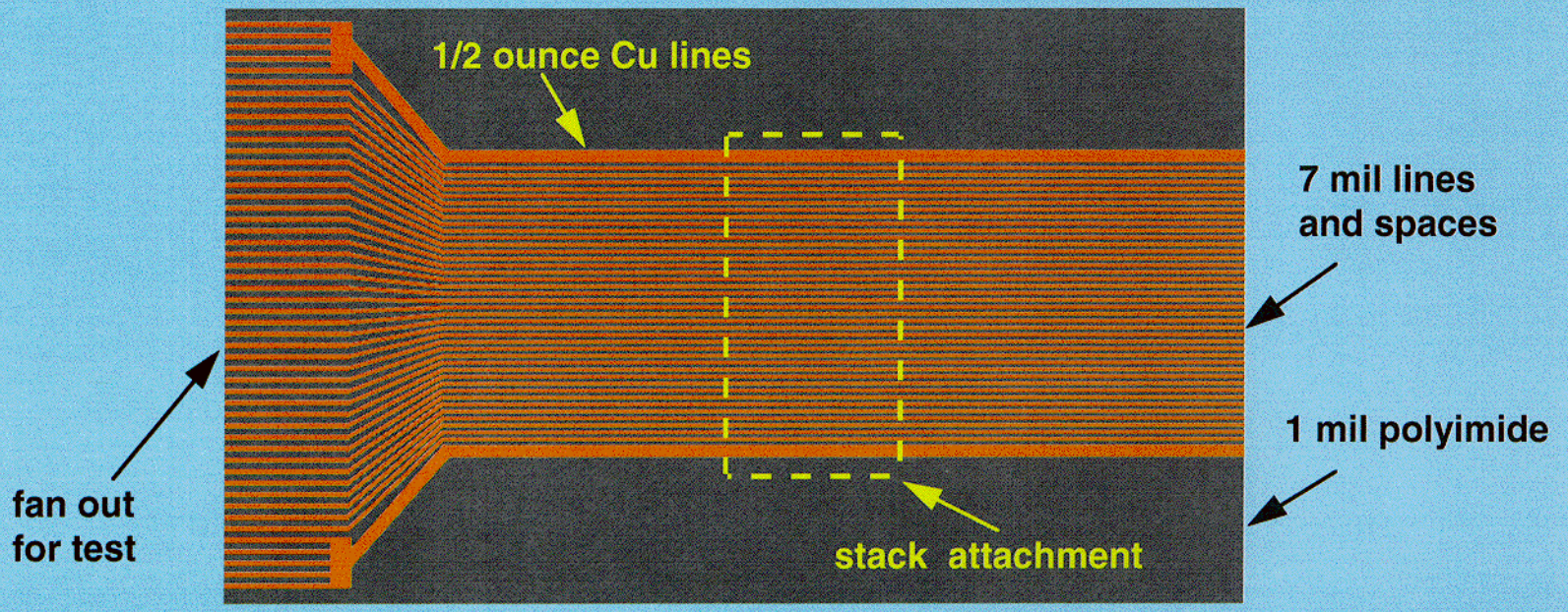
Vss bus

data and control lines

address lines

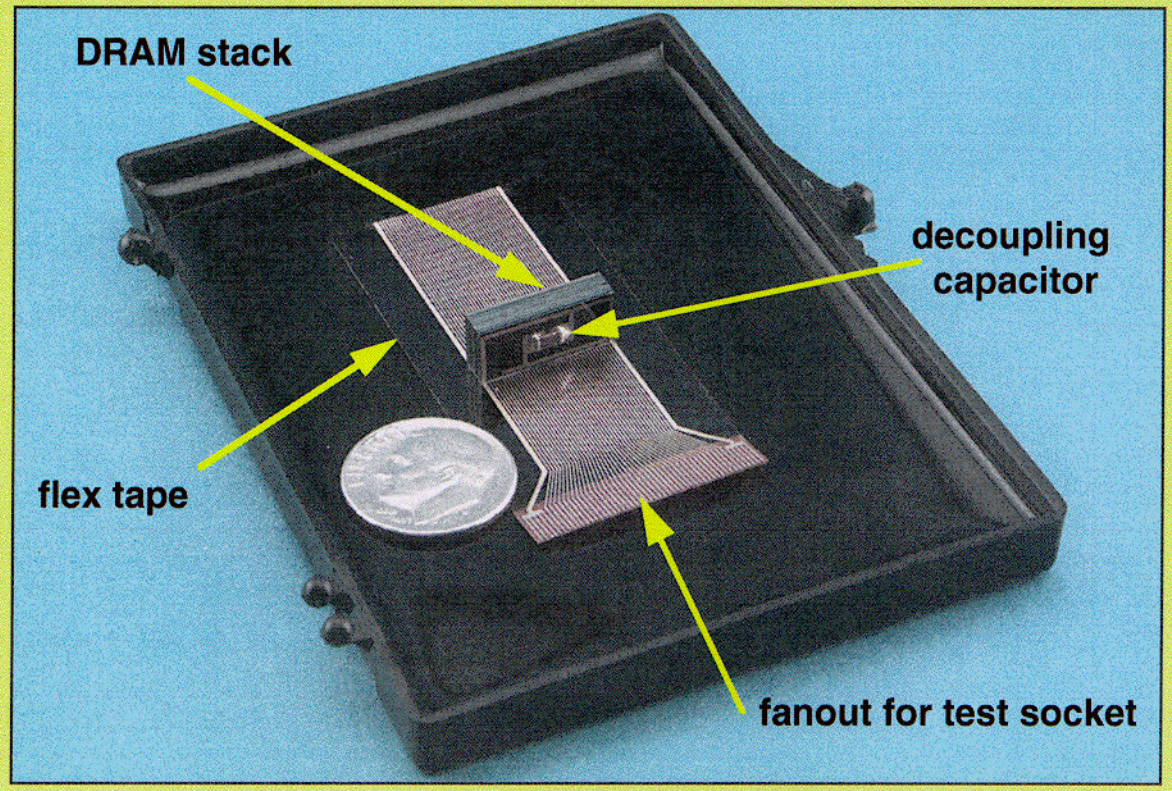
- 9 reroute patterns are used for each stack (i.e., 9 reroute files)
- Address, Vss, Vcc, and OE are routed the same for all chips
- Data, RAS, CAS, and W are routed differently for each chip

Single-sided Flex Circuit for Connecting DRAM Stack to a Printed Circuit Board

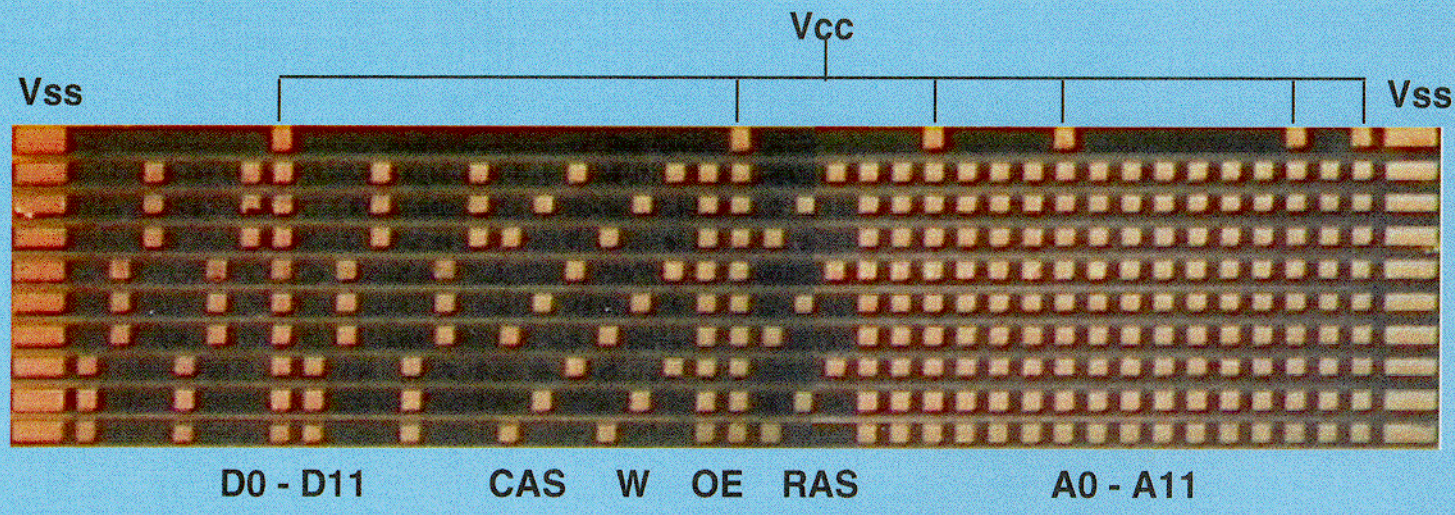


- Sufficiently transparent to allow easy alignment to pads
- Eliminates TCE mismatch problems between stack and PCB
- Simple, inexpensive attachment using Z-axis adhesive film (ZAF)
- Eliminates solder bumping and multilevel metal silicon substrates

9-Chip, 144-Mb DRAM Stack on Flex

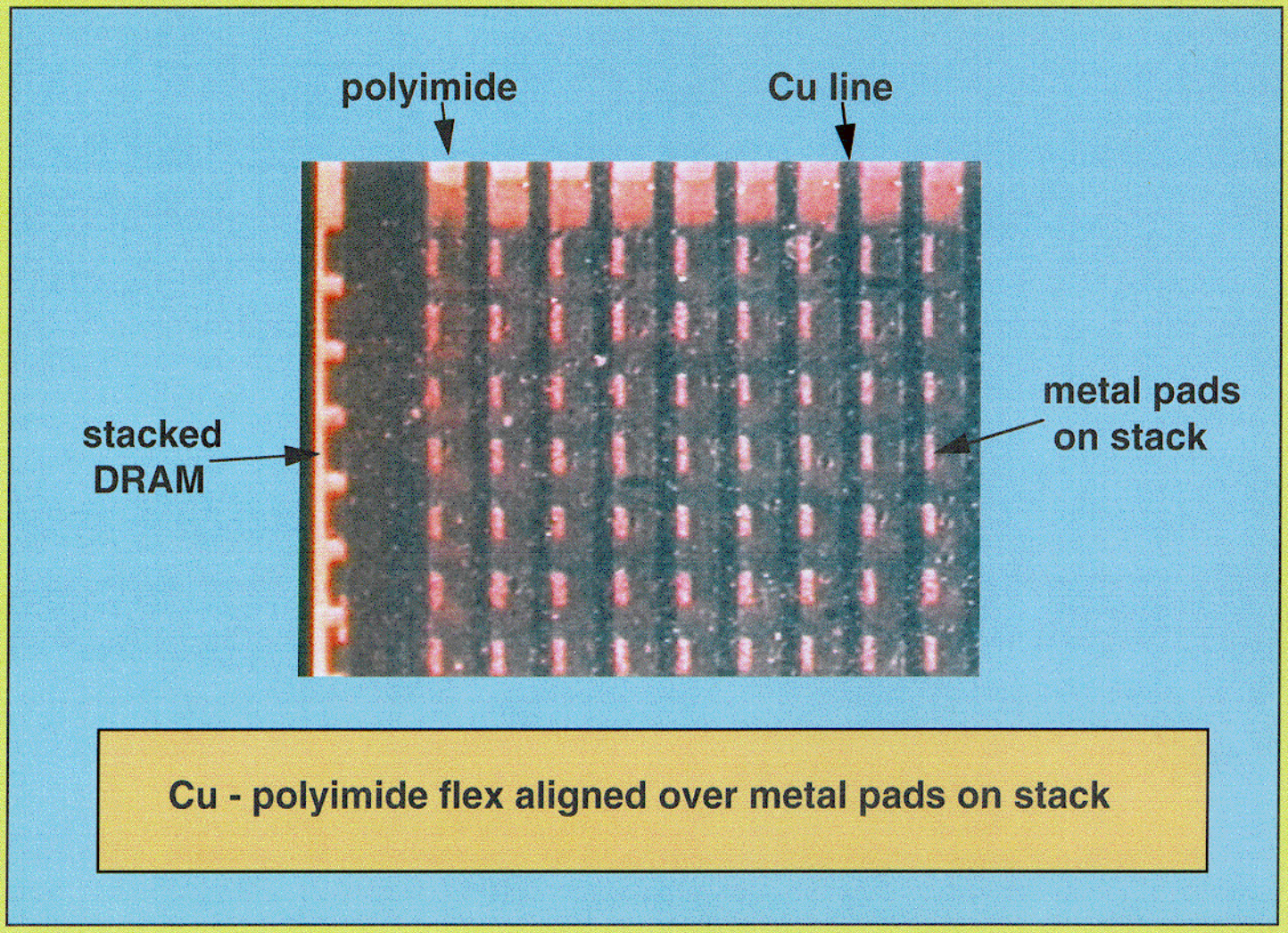


I/O Pads on the Side of a 9-DRAM Stack



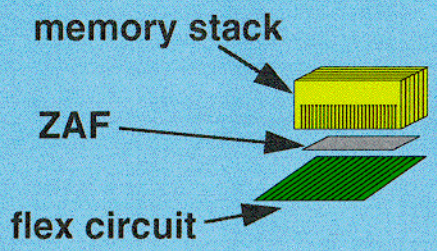
- Three chips form a cell which is 4M x 12 = 48 Mb
- Each stack has 12M x 12 = 144 Mb
- All address lines, power, ground, and OE are bussed
- Data lines from each die in a cell are bussed together
- Control lines (RAS, CAS, W) are bussed “between” cells

Alignment of Flex Circuit to Stack Pads

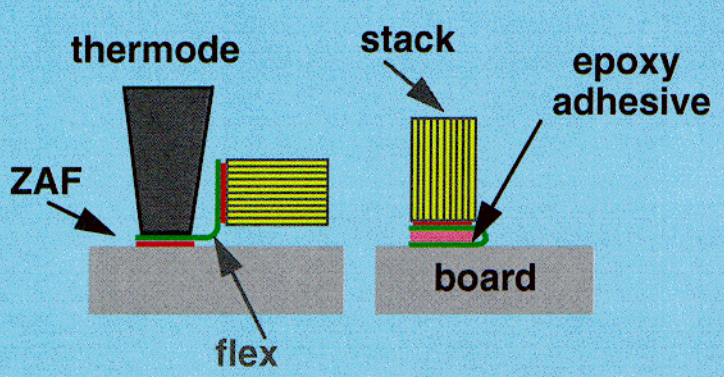


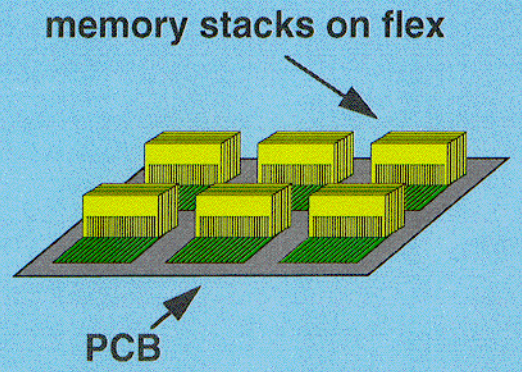
Cu - polyimide flex aligned over metal pads on stack

Z-Axis Adhesive Film Interconnections

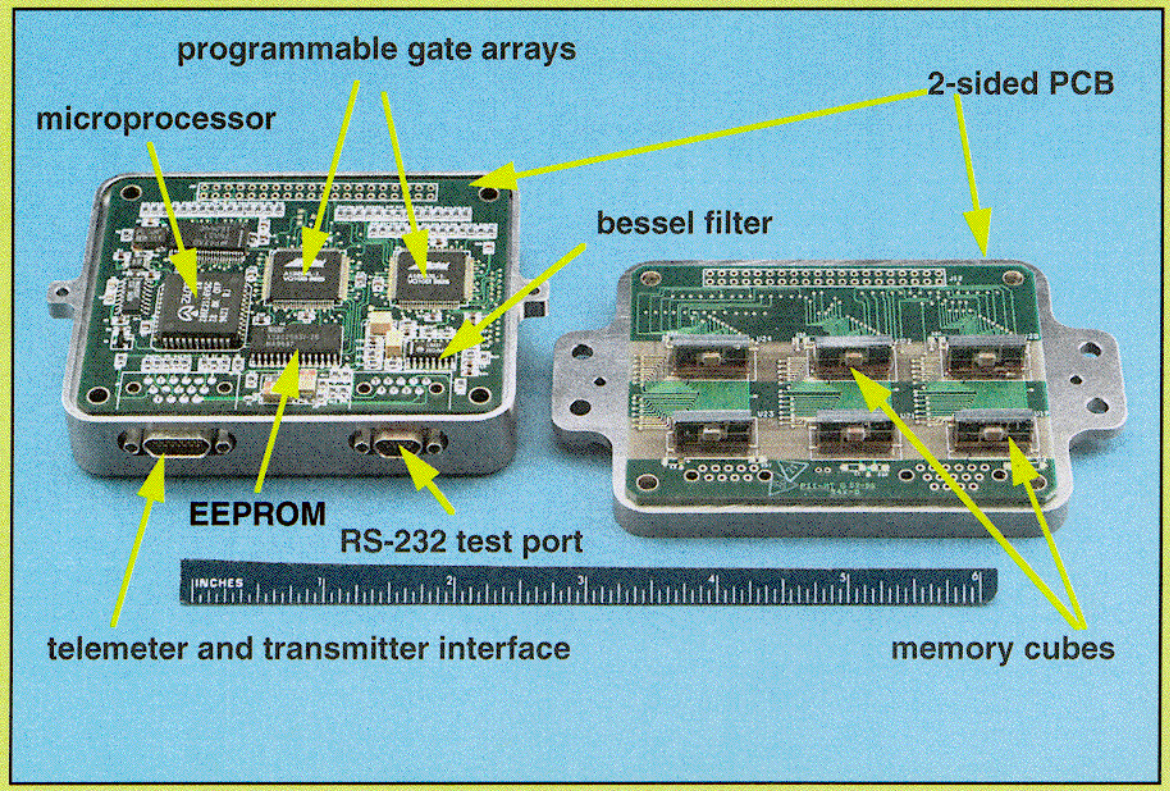


- Stack DRAMs in mechanical fixture
- Use diaphragm to connect stack to flex with Z-axis adhesive film (ZAF)
- Bond 6 memory stacks on flex to PCB with ZAF ; the flex is folded over on itself
- Use epoxy adhesive to bond the flex to itself





906 Mbit Double-Sided Memory Board



Summary

- A 906 Mb memory card has been fabricated for use in a flight test telemeter
- 3D laser patterning has been used to reroute DRAM I/O onto sidewalls
  - Angling the laser beam is key to patterning vertical surfaces
  - Electrodeposited photoresist provides conformal photoactive film on both horizontal and vertical surfaces
  - A unique pattern on each DRAM replaces pad-to-pad bonding with pad-to-line bonding, reducing packaging complexity and expense
- Single-sided flex has been used as an intermediate packaging level to eliminate TCE mismatch problems
- Z-Axis adhesive film has been used to interconnect DRAM stacks to flex, and flex to printed circuit board
- Future work - build 7.2 Gb memory with 12 stacks of 64 Mb DRAMs